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Published in:
2006 IEEE International Solid-State Circuits Conference , Digest of Technical Papers

Link to article, DOI:
10.1109/ISSCC.2006.1696108

Publication date:
2006

Document Version
Publisher's PDF, also known as Version of record

11.2 A 2.3GHz LC-Tank CMOS VCO with Optimal Phase Noise Performance

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It might appear surprising that something new can still be found about fundamental phase noise relations in LC-tank CMOS VCOs. Yet, this work demonstrates that the $1/f^2$ phase noise displayed by the current-biased VCO with double switch pair (Fig. 11.2.1, referred to hereafter as the DS-VCO) is lower than is commonly assumed. In particular, its minimum level (i.e., that caused by tank losses and switches) is 6dB below the minimum level for the LC-tank VCO with a single switch pair and center-tapped inductor (SS-VCO), when both VCOs make use of the same LC tank and bias current I_B, and both are working in the current-limited region. Such a result was already conjectured in [1], noticing that, under the above conditions, the oscillation amplitude in the DS-VCO is ideally double that in the SS-VCO. This conjecture, however, hinged on the unproven (and actually unmotivated) assumption that the two VCO cores generate an equal amount of noise (see e.g. [1], reply section). The best previous understanding of the DS-VCO was that the thermal noise in the transistors' channels dominates the $1/f^2$ phase noise [2]. Since such noise sources ideally contribute only ~40% of the total phase noise in the SS-VCO [3], it would seem that the DS-VCO cannot yield a full 6dB phase noise improvement and would, therefore, have a lower phase-noise figure-of-merit (FoM) than the SS-VCO. This conclusion may be the main reason why the DS-VCO is less popular than the SS-VCO, in spite of the lower I_B needed for a given oscillation amplitude and the well-known opportunity to achieve a low $1/f^3$ corner with a DS-VCO.

Our phase noise analysis makes use of a *symbolic* approach to Hajimiri's and Lee's impulse sensitivity function (ISF) theory [4], where the $1/f^2$ phase noise L at the angular frequency offset $\Delta\omega$ is calculated as

$$L(\Delta\omega) = 10\log\left(\sum_n \frac{\Gamma_{n,\mathrm{rms}}^2 \cdot \overline{i_n^2}/\Delta f}{2q_{\max}^2(\Delta\omega)^2}\right) \qquad (1)$$

where q_{max} is the maximum amount of signal charge loaded onto the tank capacitance C, i_n is a white current noise source, and Γ_n is the (effective) ISF for i_n. It is well-known [3,4] that, assuming a sinusoidal waveform $V(\phi) = A\sin(\phi)$ across C (with $0 \le \phi \le 2\pi$), the ISF associated with R is $\Gamma_R(\phi) = \cos(\phi)$. The symbolic expressions for the ISF for all MOS channel-current noise sources can be found in terms of the known $\Gamma_R(\phi)$ by analyzing the simplified small-signal circuit of the oscillator (Fig. 11.2.2) and applying the definition of ISF as the excess phase generated by a current impulse injected into the oscillator in parallel with the respective noise source [4]. A straightforward circuit analysis, hinging on the property that a capacitor presents infinitesimal impedance to an impulsive current, results in the ISFs given in Fig. 11.2.2. A compact formula for the $1/f^2$ phase noise is obtained using the square-law MOS current equation, and a MOS current noise $\overline{i_{\mathrm{n,n/p}}^2} = 4\,k_B\,T\,\gamma_{n/p}\,g_{m,n/p}\,\Delta f$, where γ_n (γ_p) is the channel noise factor for nMOS (pMOS) devices. Under these hypotheses, the *exact* expression for the $1/f^2$ phase noise caused by tank losses and switches is

$$L(\Delta\omega) = 10\log\left(\frac{k_B T}{A^2 C^2 (\Delta\omega)^2 R}\left(1+\frac{\gamma_n+\gamma_p}{2}\right)\right) \qquad (2)$$

where $A \approx (4/\pi)RI_B$ is the oscillation amplitude. The impact of the tail current noise can be derived in the same way as in [3].

A careful comparison with the $1/f^2$ phase noise displayed by the SS-VCO [3] shows indeed that (2) yields a ~6dB lower phase noise for the same LC-tank and I_B (6dB exactly if $\gamma_p=\gamma_n$). We notice that the noise contribution of each transistor in the DS-VCO is proportional to 1/R *independently* of the transistor transconductance, which is true in the SS-VCO as well. However, the relative impact of each transistor in the DS-VCO is only half that in the SS-VCO, and, since there are twice as many transistors in the DS-VCO, the total relative impact of the transistors is the same in both oscillators. Numerous SpectreRF simulations fully confirm these results.

Although (2) shows that nMOS and pMOS switches ideally contribute equally to phase noise, there is nevertheless an asymmetry between nMOS and pMOS pairs, due to the absence of a high impedance level at the sources of the pMOS switches (nMOS and pMOS swap of course roles if top-biasing is adopted). As a consequence, while the nMOS ISFs are independent of the capacitances C_{par} between LC-tank outputs and ground, the pMOS ISFs depend very strongly on C_{par}. A large C_{par} results in much larger pMOS ISFs (Fig. 11.2.3), and the pMOS noise rapidly becomes the dominant cause of phase noise. As an example, if half of the overall tank capacitance is parasitic, the simulated phase noise deterioration, compared to (2), is already in excess of 3dB.

It is therefore critical to keep C_{par} as small as possible, by minimizing transistor dimensions (especially pMOS), capacitances of coil and varactors to substrate, and loads presented by VCO buffers.

The DS-VCO was built in a 0.35 m CMOS process with four Al metal layers. The top layer is 2 m thick, allowing the realization of a 2.6nH inductor with a Q of ~11 at 2.3GHz. No shield under the inductor was used, in order to minimize C_{par}. Floating MIM capacitors and accumulation-MOS varactors realize the mixed-mode tuning, setting at the same time the center frequency to 2.25GHz. Open-drain buffers drive 50Ω off-chip loads. A reference SS-VCO was implemented as well, making use of an nMOS pair and of the same tank used in the DS-VCO. The phase noise induced by the tail current noise was made negligible in both VCOs.

The DS-VCO is tunable between 2.15GHz and 2.35GHz, covered in four overlapping bands of 75MHz each. Fig. 11.2.4 shows the phase noise measured as a function of I_B; the phase noise difference in favor of the DS-VCO is 5-7dB when both VCOs are working in the current-limited region, in very good agreement with the theoretical 6dB. The phase noise plot for the DS-VCO at 2.3GHz (Fig. 11.2.5) shows a phase noise of –143.9dBc/Hz at 3MHz offset, for an excellent FoM of 191.6dBc/Hz (V_{dd}=2.5V, I_B=4mA). Despite the process used, this is the highest FoM reported to date for DS-VCOs. The $1/f^3$ corner is below 250kHz. Fig. 11.2.6 shows that the DS-VCO phase noise varies by less than 1dB across the tuning range, the FoM being almost constant. Finally, the phase noise is at most only 1dB higher than the value yielded by (2), from which it can be concluded that the phase noise performance of the DS-VCO is indeed optimal. A chip photo of both VCOs is visible in Fig. 11.2.7.

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[1] H. Wang, A. Hajimiri, T. H. Lee. "Comments to "Design Issues in CMOS Differential LC Oscillators," and Authors' Reply," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 286-287, Feb., 2000.

[2] D. Ham , A. Hajimiri. "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896-909, June, 2001.

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[4] A. Hajimiri, T. H. Lee. "A General Theory of Phase Noise in Electrical Oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179-194, Feb., 1998.

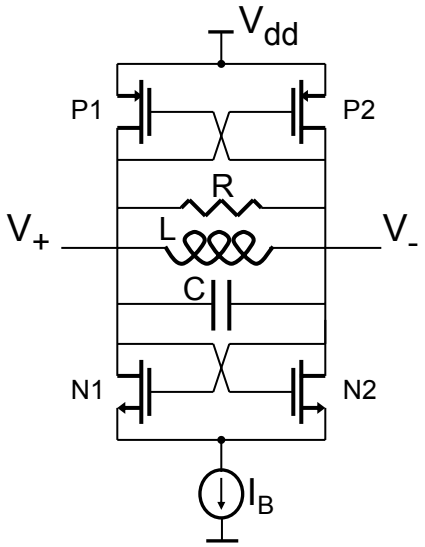
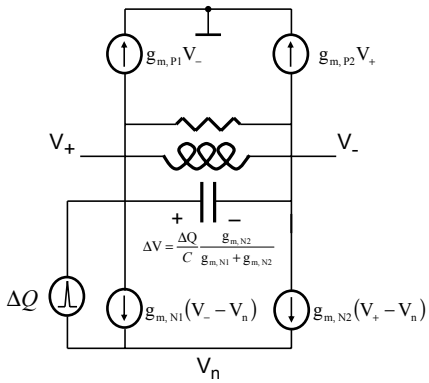


Figure 11.2.1: Simplified schematic view of the DS-VCO.



$$\Gamma_R = \cos(\phi)$$

$$\Gamma_{N1} = \Gamma_R \frac{g_{m,N2}}{g_{m,N1}+g_{m,N2}}$$

$$\Gamma_{N2} = \Gamma_R \frac{g_{m,N1}}{g_{m,N1}+g_{m,N2}}$$

$$\Gamma_{P1} = \Gamma_R \frac{g_{m,P2}}{g_{m,P1}+g_{m,P2}}$$

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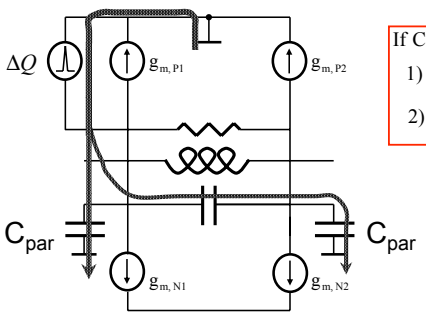
Figure 11.2.2: Left: small-signal circuit for phase noise calculations (as an example, the impulsive current source in parallel to N1 is used to derive the ISF for N1). Right: expressions of all relevant ISFs (all transconductances are functions of ϕ).



If $C_{par} >> C$:

1) Γ_{N1} and Γ_{N2} are unchanged

2) $\Gamma_{P1} = \Gamma_{P2} \approx \frac{\Gamma_R}{2}$ (much larger)

Figure 11.2.3: The symmetry between nMOS and pMOS pairs is broken when C_{par} is non-negligible. If C_{par} is large, pMOS-induced phase noise becomes dominant.

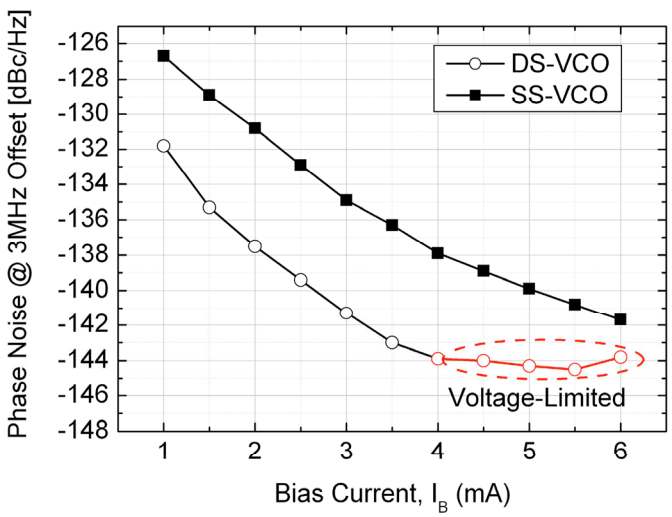


Figure 11.2.4: Current-limited phase noise of SS-VCO and DS-VCO at 3MHz frequency offset, as a function of bias current.

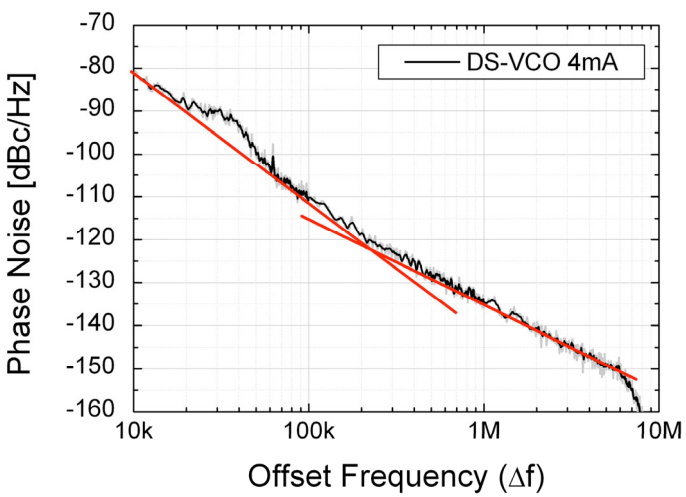


Figure 11.2.5: Phase noise plot for the DS-VCO (f_{osc}=2.3GHz, V_{dd}=2.5V, I_B=4mA).

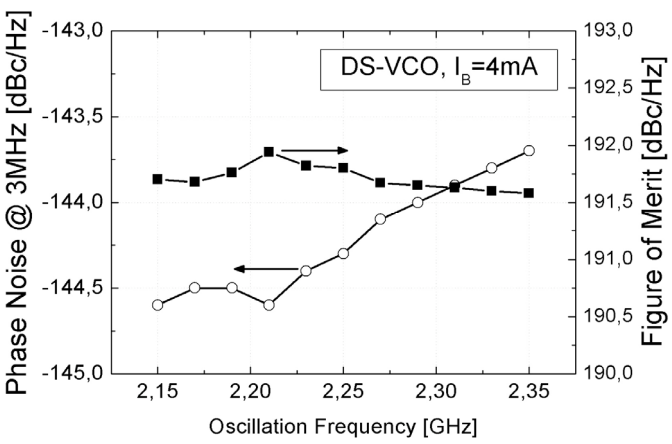
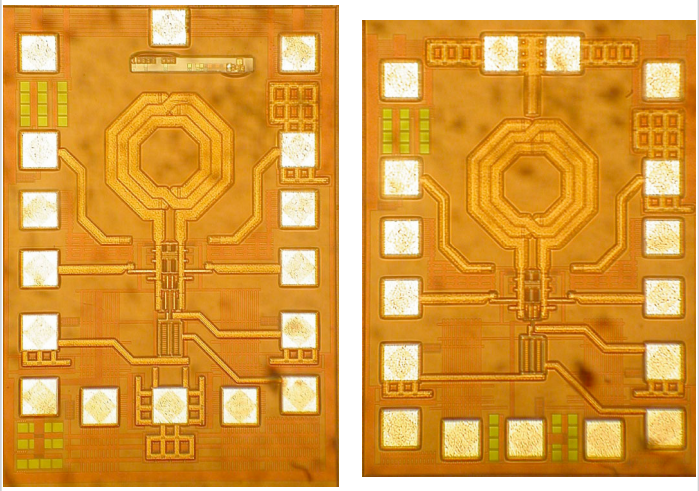


Figure 11.2.6: Phase noise and FoM for the DS-VCO at 3MHz frequency offset across the tuning range (V_{dd}=2.5V, I_B=4mA).



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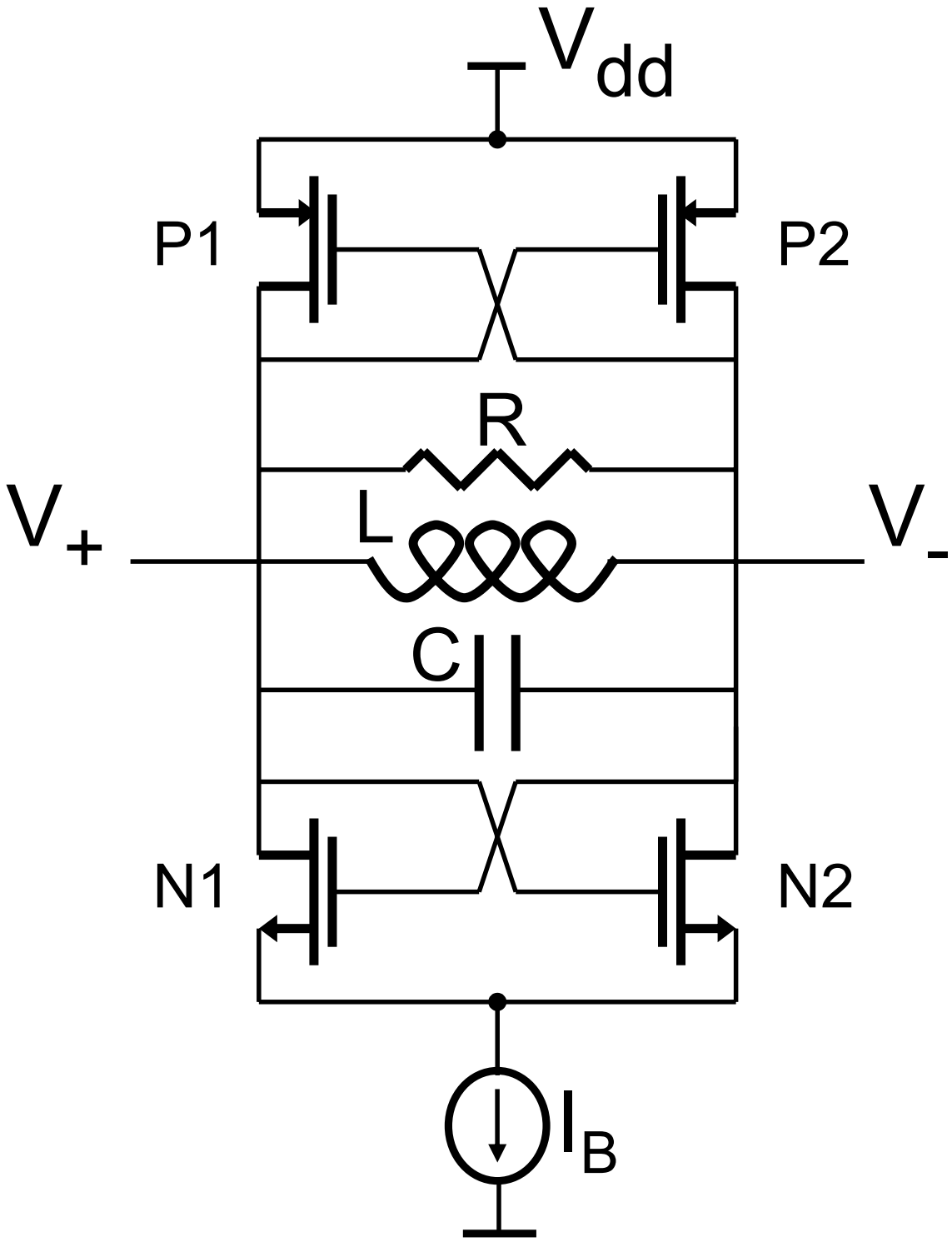

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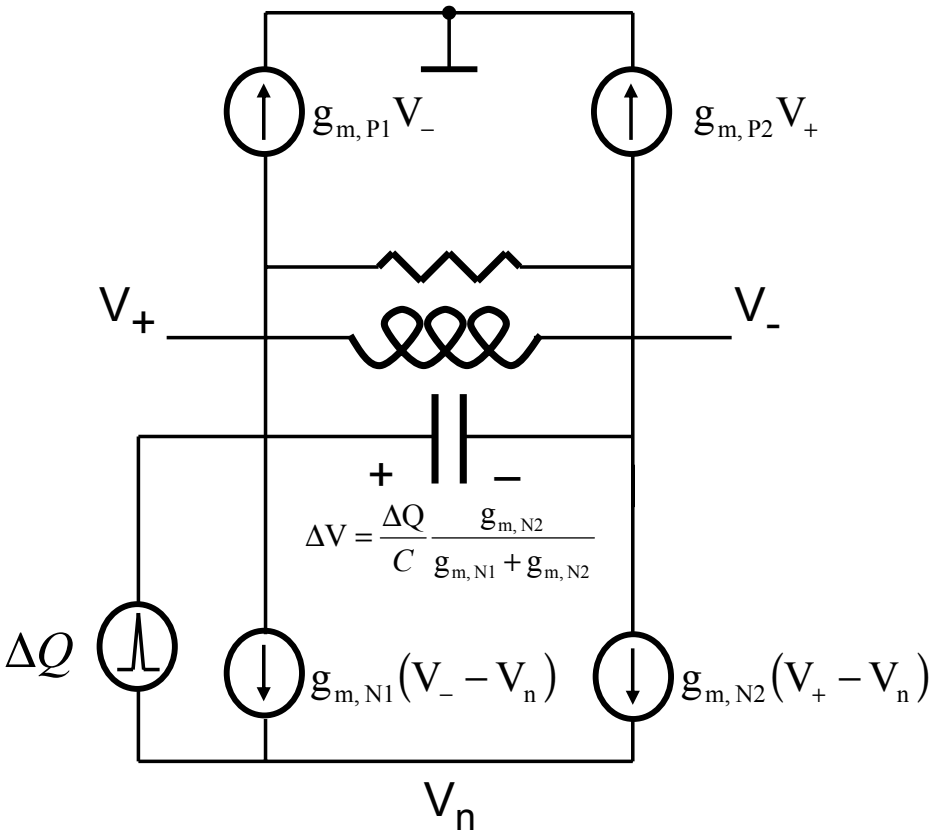

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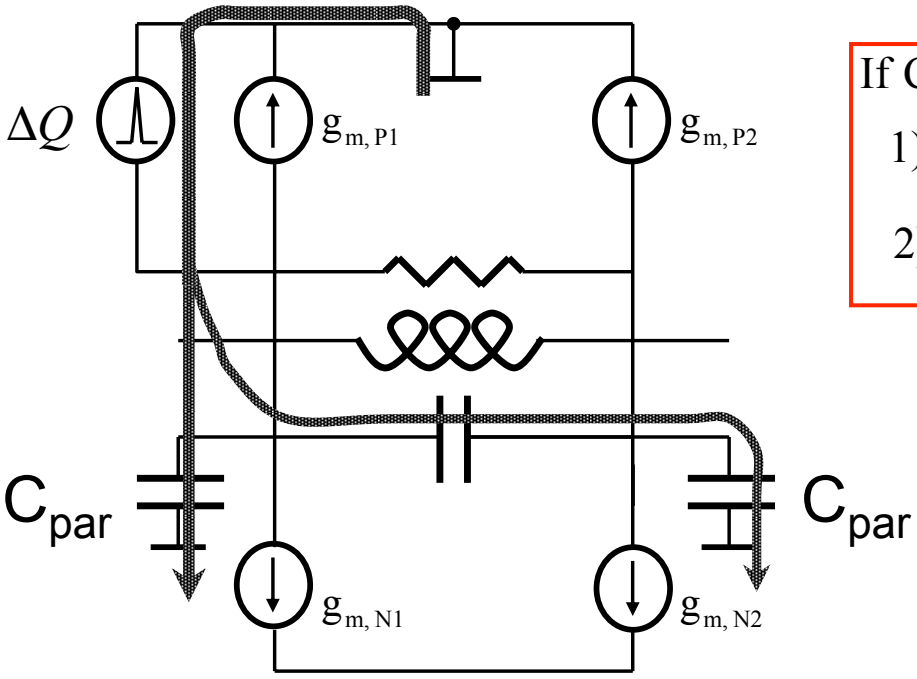

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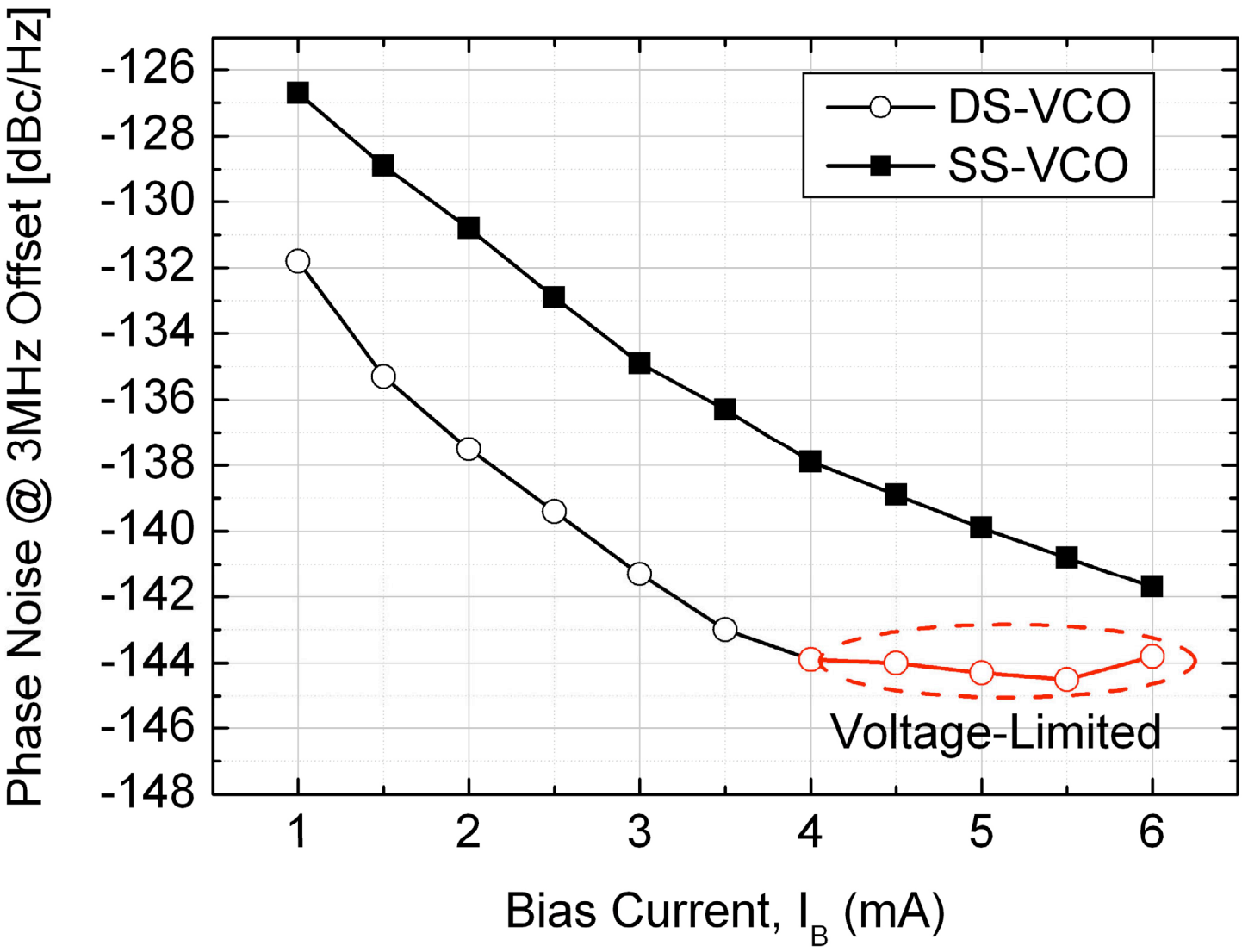

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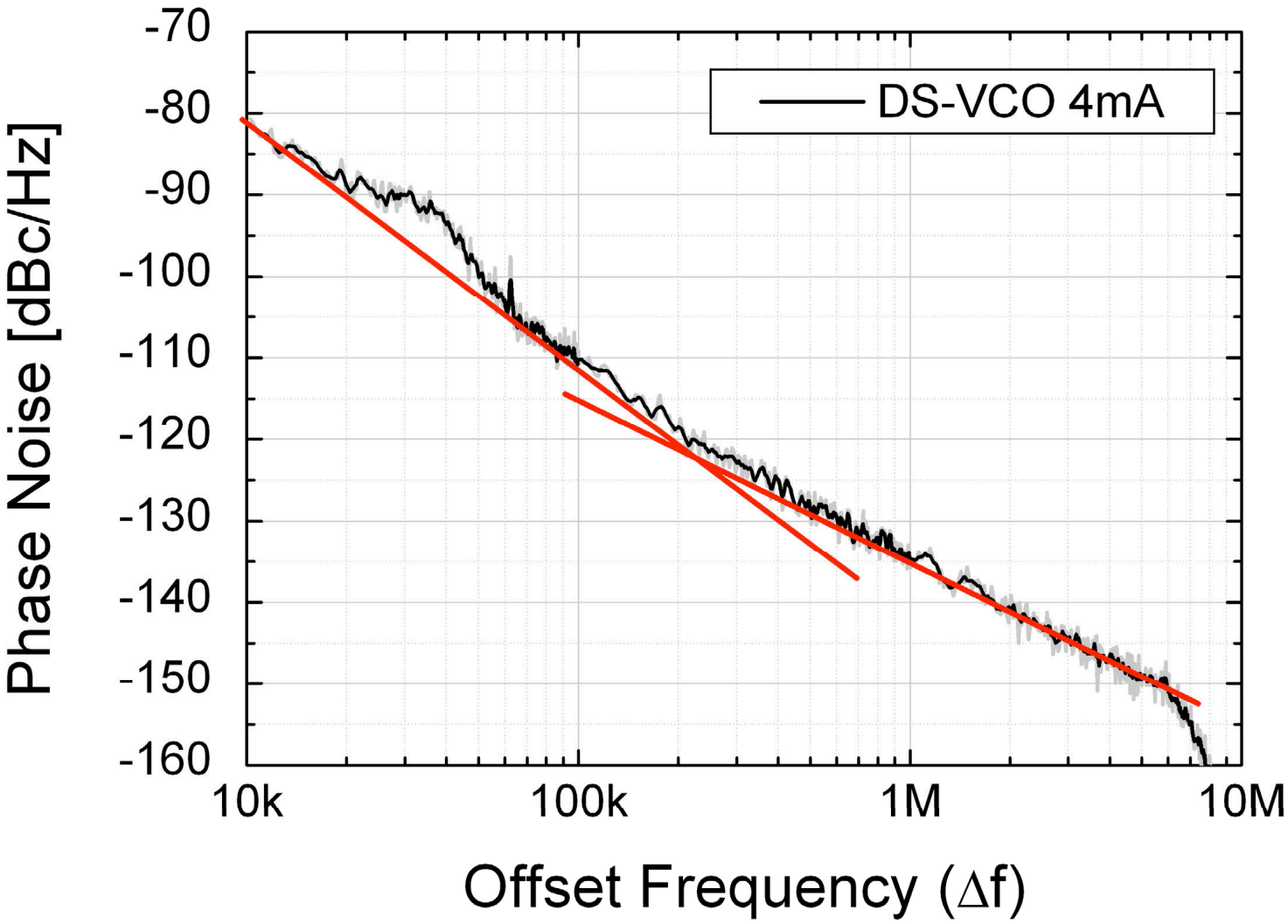

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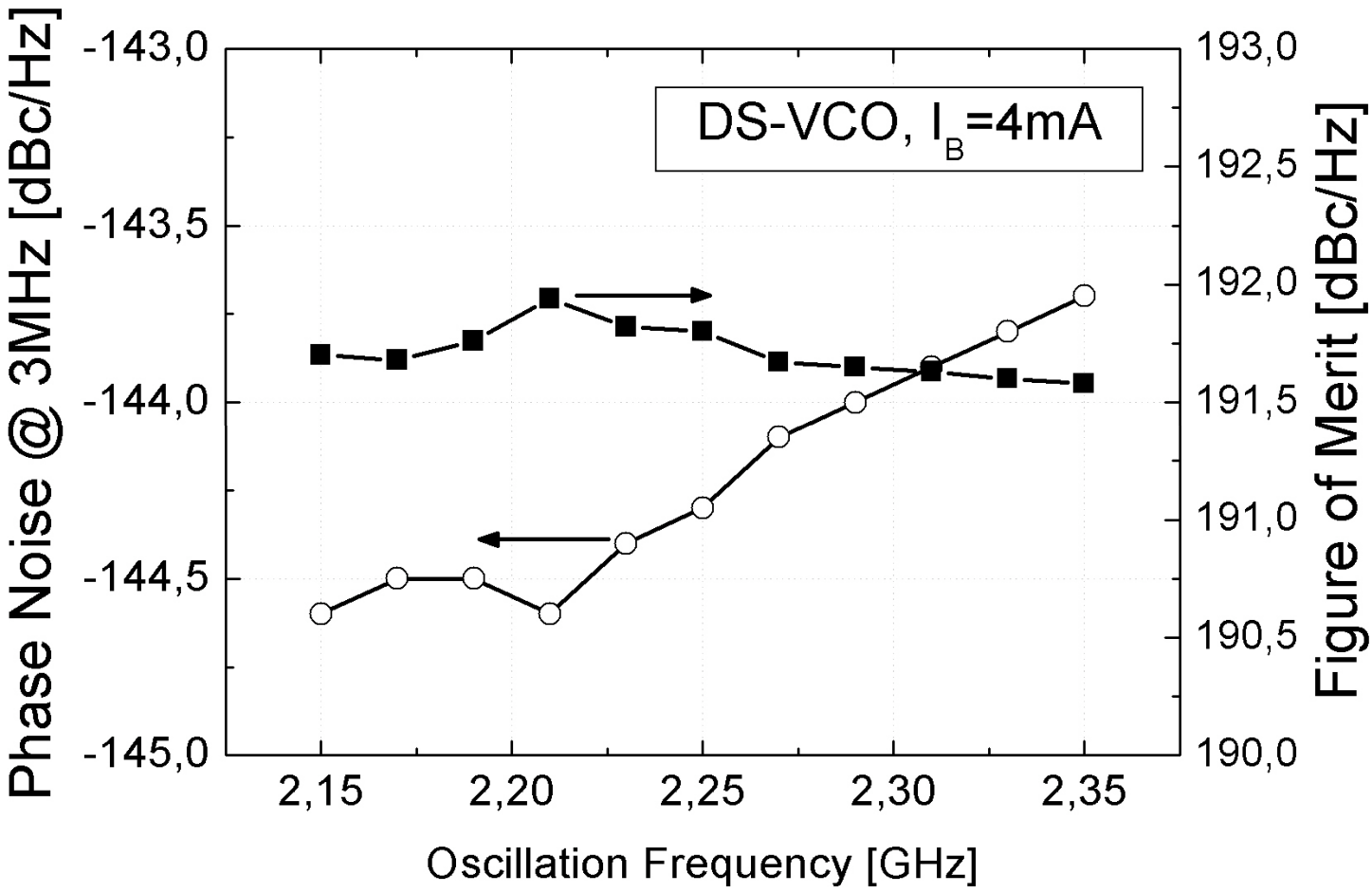

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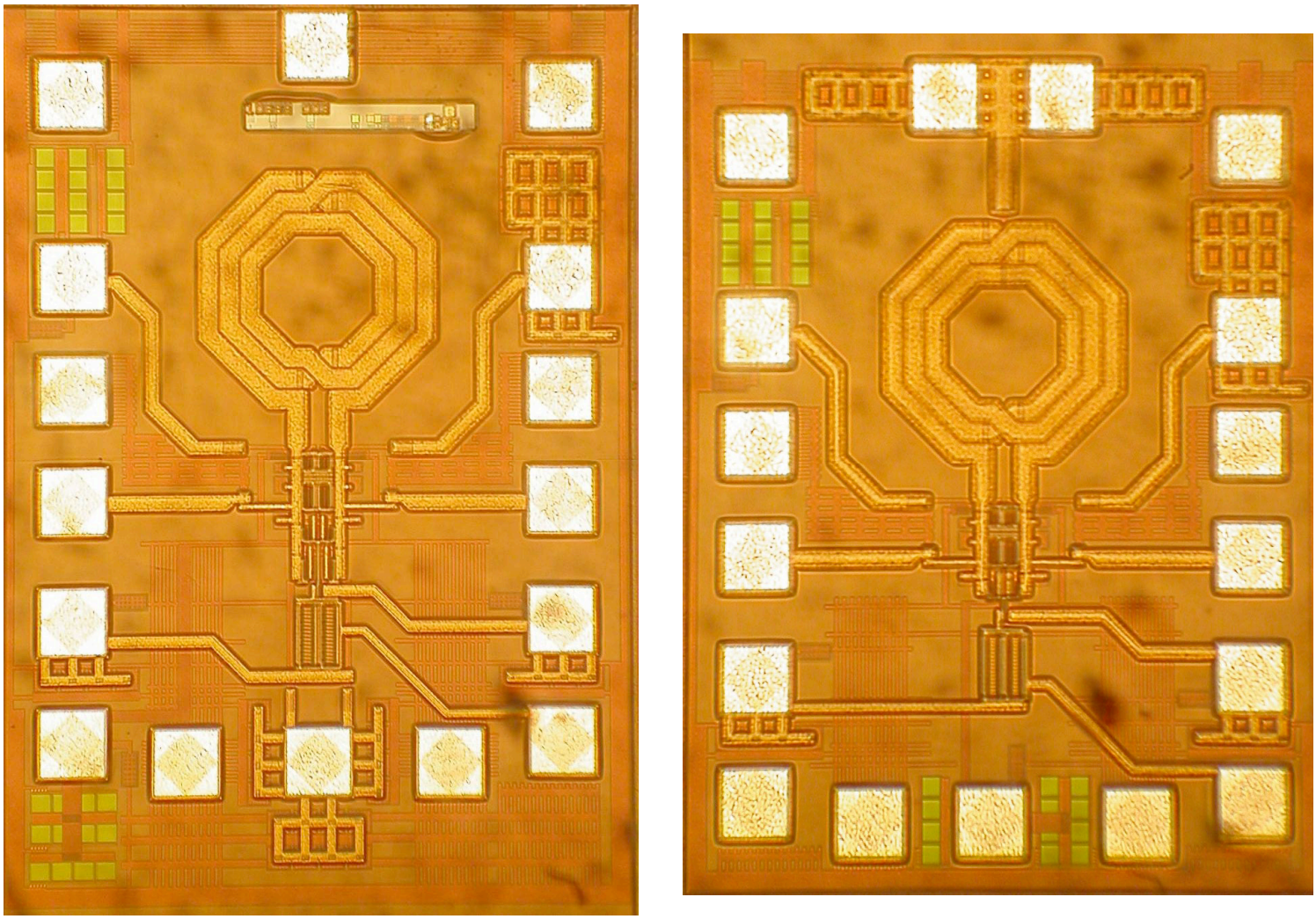

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